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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,285	03/16/2005	Stephen J. Battersby	GB02 0152 US	6607

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
370 W. TRIMBLE ROAD MS 91/MG
SAN JOSE, CA 95131

EXAMINER	
CHOW, YUK	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,285	BATTERSBY ET AL.	
	Examiner	Art Unit	
	Yuk C. Chow	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-18 and 21-25* is/are rejected.

7)☒ Claim(s) *10-12, and 19-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not state that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to **patentability** as defined in 37 CFR 1.56.

Drawings

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 11 is objected to because of the following informalities: improper dependency, claimed limitations in claim 11 can be found in claim 10, not in claim 2. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "**5 bit digital word**" in claim 6 is used by the claim to mean "5-bit input data", while the accepted meaning is "5-bit binary data." The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-9, 13-18 and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Sekine (US 2003/0146896 A1).

As to claim 1, Sekine discloses an active matrix display, comprising:

an array of pixels provided over a common substrate (see [0011]), each pixel comprising a display element and a switching device (see Fig. 2 and [0017]); and

a column driver (Fig. 2(20)) for providing signals to the pixels for driving the display elements (see [0051]), the column driver comprising digital to analogue converter circuitry (see Fig. 2(10)) and providing a first number of display element drive levels greater than 2, wherein each pixel comprises means for converting the first number of display element drive levels (Fig. 8(Vcs1)) into a second, greater number, of pixel grey levels (Fig. 8(Vcs2) also see [0062]-[0067]).

As to claim 2, Sekine discloses a display as claimed in claim 1, wherein the means for converting comprises, within each pixel, at least first and second display elements having different areas (See Fig. 2(PXTFT) of GO1 and GE1).

As to claim 3, Sekine discloses a display as claimed in claim 2, wherein the first and second display elements have areas in the ratio 1:2 (It's inherently to choose different ratio to have different level of grey scale).

As to claim 4, Sekine discloses a display as claimed in claim 1, wherein the means for converting comprises, within each pixel, charge redistribution circuit elements (See Fig. 6(GO, GE)).

As to claim 5, Sekine discloses a display as claimed in claim 4, wherein the charge redistribution elements comprise two display elements (Fig. 6(GO1, GE1)), an input switch (Fig. 2(SWD)) between the input to the pixel and a first display element and a charge redistribution switch (Fig. 2(SWR)) between the first and second display elements (see [0058]-[0060]).

As to claim 6, Sekine discloses a display as claimed in claim 1, wherein the digital to analogue circuitry receives a 5 bit digital word (see [0086], multi-bit DAC).

As to claim 7, Sekine discloses a display as claimed in claim 6, wherein the output of the digital to analogue circuitry comprises a number of levels less than 32 (It's inherent that 5-bit input could have 32 possible levels).

As to claim 8, Sekine discloses a display as claimed in claim 7, wherein the output digital to analogue circuitry comprises 22 possible levels (It's possible that 5-bit input could have 22 levels).

As to claim 9, Sekine discloses a display as claimed in claim 1 further comprising a converter for deriving from a 6 bit drive signal (see [0061]) a signal for selecting which one or ones of the first number of levels to apply to each display element (Fig. 2(SWV) also [0060]-[0061]).

As to claim 13, Sekine discloses a display as claimed in claim 1, comprising a plurality of row conductors (Fig. 2(GO, GE)), a number of row conductors being associated with each row of pixels corresponding to the number of display elements within each pixel (see [0089]).

As to claim 14, Sekine discloses a display as claimed in claim 1, wherein each pixel comprises a memory element (Fig. 4(MEM)) for storing digital drive values for the display elements of each pixel (see [0052]).

As to claim 15, Sekine discloses a display as claimed in claim 1, wherein the digital to analogue circuitry is provided on the common substrate (see [0011]).

As to claim 16. A display as claimed in claim 15, wherein the pixel array and the digital to analogue circuitry are formed using low temperature polysilicon processing (It's known in the art that a TFT having a polysilicon layer is produced by a low temperature process, typically via a laser annealing procedure).

As to claim 17, Sekine discloses a method of driving an active matrix display, comprising:

providing first (Fig. 8(Vcs1)) and second drive voltages (Fig. 8(Vcs2) to a display pixel having first and second display elements, the first and second drive voltages being selected from two adjacent drive voltage levels of a digital to analogue converter which has more than 2 output levels (Fig. 3(SP1, SP2)); and

within the pixel, generating an intermediate grey level corresponding to a drive voltage between the first and second levels (see [0062]-[0067]).

As to claim 18, Sekine discloses a method as claimed in claim 17, wherein the first display element has a first area and the second display element has a second area different to the first area, area weighting being used to generate the intermediate grey level (see [0062]-[0067]).

As to claim 21, Sekine discloses a method as claimed in any one of claim 18, wherein a plurality of sub-rows of pixels are addressed in turn, each sub-row comprising respective display elements for each pixel (see [0082]-[0084]).

As to claim 22, Sekine discloses a method as claimed in any one of claim 18, wherein a plurality of rows of pixels are addressed in turn, each row being addressed

once to address both display elements and a second time to readdress the second display element (see [0082]-[0084]).

As to claim 23, Sekine discloses a method as claimed in claim 17, wherein charge sharing between the display elements is used to generate the intermediate grey level (It's inherently to share charge between different display elements to have different level of grey scale).

As to claim 24, Sekine discloses a method as claimed in claim 23, wherein the first and second drive voltages are provided by a digital to analogue converter which receives a 5 bit input (see [0086], multi-bit DAC).

As to claim 25, Sekine discloses a method as claimed in claim 24, wherein the drive voltages are provided from a column driver circuit integrated onto the active plate of the active matrix display (See Fig. 2, [0011] and [0051]-[0055]).

Allowable Subject Matter

8. Claims 10-12, 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: cited references do not teach or mention applicant's claimed limitation, divider for dividing by 3 and providing a divisor and remainder in claim 10 and 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuk C. Chow whose telephone number is 571 270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YC
01/22/2008

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER